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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/052,736	01/23/2002	Satoshi Ikeda	SON-2313	3283

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EXAMINER

KERVEROS, JAMES C

ART UNIT PAPER NUMBER

2133

DATE MAILED: 06/17/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/052,736

Applicant(s)

IKEDA, SATOSHI

Examiner

JAMES C. KERVEROS

Art Unit

2133

~ The MAILING DATE of this communication appears on the cover sheet with the correspondence address ~

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 30 March 2005.
- 2a) ☐ This action is FINAL. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 3 and 6-32 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 3 and 6-32 is/are rejected.
- 7) ☒ Claim(s) 3 and 6-21 is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 13 January 2002 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____

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DETAILED ACTION

In view of the Appeal Brief filed on 3/30/2005, PROSECUTION IS HEREBY REOPENED. A new ground of rejection is set forth below.

To avoid abandonment of the application, appellant must exercise one of the following two options:

(1) file a reply under 37 CFR 1.111 (if this Office action is non-final) or a reply under 37 CFR 1.113 (if this Office action is final); or,

(2) request reinstatement of the appeal.

If reinstatement of the appeal is requested, such request must be accompanied by a supplemental appeal brief, but no new amendments, affidavits (37 CFR 1.130, 1.131 or 1.132) or other evidence are permitted. See 37 CFR 1.193(b)(2).

This is a Non-Final Office Action in response to Amendment and Appeal Brief filed 3/30/2005.

Claims 1, 3, 4 and 5 are cancelled. Claims 3 and 6-32 are currently pending in this application, with claims 3, 6 and 22 being independent.

Prior Office Action Withdrawals

Objection to the abstract of the disclosure is hereby withdrawn in view of the Amendment to the Abstract as suggested by the Examiner.

Objection to the specification under 37 CFR 1.71 in reference to the limitation "the set information" is hereby withdrawn in view of Applicant's arguments.

Rejection of Claim 3 under 35 U.S.C. 112, first and second paragraph, in reference to the limitation "the set information" is hereby withdrawn in view of Applicant's arguments.

Claim Objections

Claims 3, 6-21 are objected to because of the following informalities:

Independent Claims 3, 6 and some associated dependent claims in passim recite: "adapted to ..." It has been held that the recitation that an element is "adapted to" perform a function is not a positive limitation but only requires the ability to so perform. It does not constitute a limitation in any patentable sense. *In re Hutchison*, 69 USPQ 138.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claim 3 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Regarding claim 3, the phrase "such a manner" renders the claim indefinite because it is unclear whether the limitations following the phrase are part of the claimed invention. See MPEP § 2173.05(d).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 3 and 6-32 are rejected under 35 U.S.C. 103(a) as being unpatentable over Satoh (U.S. Patent No. 6,477,672) in view of Kurosaki (U.S. Patent No. 6,314,536).

Regarding independent Claim 3, Satoh substantially discloses a semiconductor testing apparatus for testing a memory under test (MUT) Figure 9, wherein a pattern generator (PG) outputs test pattern data to be applied to the input of memory under test (MUT) through waveform formatter FC and drivers DR in accordance with the stored pattern generating sequence, and an output signal obtained from the (MUT) through the voltage comparator VCP is inputted to the logical comparator LOC where it is compared with an expected value pattern data (signal) EXP supplied from the pattern generator PG to determine whether or not the memory under test MUT has outputted a normal response signal, comprising:

Test pattern memory means, (test program 101) storage area in the (controller 100) for storing test pattern data created by a user (programmer), and upon a test start instruction given from the controller 100, the pattern generator PG outputs test pattern

data to be applied to the memory under test (MUT) in accordance with the stored pattern generating sequence described in the test program 101.

Test pattern generation means (pattern generator PG) for generating a test pattern signal on the basis of the (test program 101) outputted from the test pattern memory means in the controller 100. A pattern generating sequence described in the test program stored in the controller 100 is previously stored in the pattern generator PG prior to the start of a test. When a test start instruction is given from the controller 100, the pattern generator PG outputs test pattern data to be applied to the memory under test MUT in accordance with the stored pattern generating sequence.

Control means (controller 100) for controlling the (test program 101) and the (pattern generator PG), where the test pattern signal based on the test pattern data of a desired address (ADR) from the (PG) can be generated at a predetermined timing according the timing generator TG, which has timing data previously stored therein prior to the start of a test, being described in the test program stored in the controller 100 and outputted for every test period. The timing generator TG outputs a clock pulse (a timing pulse) for each test period in accordance with the stored timing data. The control means (controller 100) controls the timing of generation of the test pattern.

Satoh does not explicitly disclose, a "cycle period rate to execute the test pattern of the desired address becomes a cycle period narrower than a predetermined rate".

However, Kurosaki (US 6,314,536), in analogous art, discloses a burst address producing circuit (8, Figure 1) capable of producing two burst address signals in one test period, which comprises a clock-repetition-rate doubling circuit 15 for outputting a

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clock at twice the pulse repetition rate of the test period signal TI, (see, Abstract). A timing chart showing waveforms and address signals produced in main elements of the memory testing apparatus 1 is illustrated in Figure 5. For example, Figure 5A shows a test period signal TI, and Figure 5D shows the burst address signals, having two burst address signals with respect to test period signal TI. Therefore, the cycle period rate of Figure 5D is narrower than the test period signal TI, by a factor of two.

It would have been obvious to a person having ordinary skill in the art at the time the invention was made to use the burst address producing circuit as taught by Kurosaki in the semiconductor testing apparatus of Satoh, for the purpose of testing a memory in the form of semiconductor integrated circuit, which adopts double data rate system and operates in burst mode, thus avoiding some of the drawbacks associated with the conventional memory testing, resulting in reduction of the throughput, and imposing heavy burden or load on programmers. The double data rate system provides a memory testing capable of supplying two address signals to a failure analysis memory in one test period, and hence capable of carrying out the test of memories at one time or within a shorter time period even in testing memories each operating in burst mode.

Regarding independent Claim 6, Satoh substantially discloses a semiconductor testing apparatus for testing a memory under test (MUT) Figure 9, comprising:

Control means (controller 100) for controlling the timing generator TG and the pattern generator PG, for generating a timing signal (Test Period) and an address

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(ADDR) signal according to a pattern generating sequence described in the test program 101 stored in the main controller 100.

Test pattern memory means, (test program 101) storage area in the (controller 100) for storing test pattern data created by a user (programmer), and upon a test start instruction given from the controller 100, the pattern generator PG outputs test pattern data to be applied to the memory under test (MUT) in accordance with the stored pattern generating sequence described in the test program 101.

Test pattern generation means (pattern generator PG) for generating a test pattern signal on the basis of the (test program 101) outputted from the test pattern memory means in the controller 100. A pattern generating sequence described in the test program stored in the controller 100 is previously stored in the pattern generator PG prior to the start of a test. When a test start instruction is given from the controller 100, the pattern generator PG outputs test pattern data to be applied to the memory under test MUT in accordance with the stored pattern generating sequence.

Satoh does not explicitly disclose a variable test pattern cycle period.

However, in analogous art, Kurosaki (US 6,314,536) discloses a clock-repetition-rate doubling circuit 15 for outputting a clock at twice the pulse repetition rate of the inputted clock including a variable delay circuit 13, which delays a clock or test period signal TI from the timing generator 7 by a time interval equal to half of one test period, Figure 1.

It would have been obvious to a person having ordinary skill in the art at the time the invention was made to use the variable delay circuit 13 as taught by Kurosaki in the

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apparatus of Satoh, for the purpose of varying the pattern Test Period, since varying the Test Period provides a memory testing capable of supplying two address signals to a failure analysis memory in one test period, and hence capable of carrying out the test of memories at one time or within a shorter time period even in testing memories each operating in burst mode.

Regarding independent Claim 22, Satoh substantially discloses a semiconductor testing method for testing a memory under test (MUT) Figure 9, comprising:

Generating a timing signal having a test pattern cycle period, using timing generator TG, which has timing data described in the test program stored in the main controller 100 and outputted for every test period. The timing generator TG outputs a clock pulse (a timing pulse) for each test period in accordance with the stored timing data, Figure 9.

Generating an address (ADR), using pattern generator PG, which outputs a test pattern data having an address signal (ADR) to be supplied to both the memory under test MUT and the failure analysis memory AFM.

Storing a first test pattern corresponding, for example, to ADR0, BLOCK No. 1 of memory under test MUT, Figure 2, within the (test program 101) storage area in the (controller 100).

Outputting the first test pattern ADR0, BLOCK No. 1 from the (test program 101) storage area in response to a test start instruction given from the controller 100, the

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pattern generator PG outputs test pattern data to be applied to the memory under test (MUT) in accordance with the stored pattern generating sequence described in the test program 101.

Combining the first test pattern ADR0, BLOCK No. 1 from the (test program 101) storage area with the timing generator TG in the pattern generator PG to generate an input test pattern signal, where the memory under test MUT receives the input test pattern signal; and

Comparing using (logical comparator LOC) to determine whether or not the memory under test MUT has outputted a normal response signal, by comparing the output signal of the voltage comparator VCP received from the memory under test MUT with an expected value pattern data (signal) EXP supplied from the pattern generator PG.

Satoh does not explicitly disclose, "varying the duration of the test pattern cycle period". However, in analogous art, Kurosaki (US 6,314,536) discloses a clock-repetition-rate doubling circuit 15 for outputting a clock at twice the pulse repetition rate of the inputted clock including a variable delay circuit 13, which delays a clock or test period signal TI from the timing generator 7 by a time interval equal to half of one test period, Figure 1.

It would have been obvious to a person having ordinary skill in the art at the time the invention was made to use the variable delay circuit 13 as taught by Kurosaki in the apparatus of Satoh, for the purpose of varying the pattern Test Period, since varying the Test Period provides a memory testing capable of supplying two address signals to

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a failure analysis memory in one test period, and hence capable of carrying out the test of memories at one time or within a shorter time period even in testing memories each operating in burst mode.

Regarding Claim 7, Satoh discloses decision means (logical comparator LOC) to determine whether or not the memory under test MUT has outputted a normal response signal, by comparing the output signal of the voltage comparator VCP received from the memory under test MUT with an expected value pattern data (signal) EXP supplied from the pattern generator PG

Regarding Claim 8, Satoh does not explicitly disclose "wherein the control means varies the duration of the test pattern cycle period". However, in analogous art, Kurosaki (US 6,314,536) discloses means for varying the duration of the test pattern cycle period, as described in the independent claim 6, above, including the obvious and motivational reasons as applied to independent claim 6.

Regarding Claim 9, Satoh discloses the first test pattern, which is part of the (test program 101) stored in the test pattern memory means (controller 100) corresponding to an address (ADDR).

Regarding Claim 10, Satoh discloses semiconductor device (memory under test MUT), which is tested during the test pattern cycle period, by outputting the timing data, described in the test program stored in the main controller 100, every test period.

Regarding Claims 11, 23, Satoh discloses wherein the control means (controller 100) receives set information (test program 101) to generate the timing signal (Test

Period) and the address (ADDR) by controlling the timing generator TG and the pattern generator PG, wherein the test program 101 specifies the duration of the (Test Period).

Regarding Claim 12, Satoh discloses timing generator TG has timing data previously stored therein prior to the start of a test, the timing data being described in the test program 101 stored in the main controller 100 and outputted for every test period.

Regarding Claim 13, 24, Satoh does not explicitly disclose, "test pattern cycle period is narrowed by varying said set information".

Regarding Claim 14, 25, Satoh does not explicitly disclose, "test pattern cycle period is widened by varying said set information".

Regarding Claims 13, 14, 24, 25, in analogous art, Kurosaki (US 6,314,536) discloses a variable delay circuit 13, which delays (narrowing) a test period signal TI, and an address hold circuit 9, which holds (widening) the first address signal ADR0 as shown in Figure 2D until a next address signal is supplied, Figure 1.

It would have been obvious to a person having ordinary skill in the art at the time the invention was made to use the variable delay and hold circuits as taught by Kurosaki in the apparatus of Satoh, for the purpose of narrowing or widening the pattern Test Period, since varying (narrowing or widening) the Test Period results in memory testing flexibility by providing a faster or slower clock for external test system compatibility.

Regarding Claim 15, 26, Satoh discloses wherein said test pattern memory means (test program 101) storage area in the (controller 100) stores a plurality of test

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patterns of the (test program 101), which is outputted from the test pattern memory means in response to the address and test period upon command from the (controller 100).

Regarding Claims 16-18, 27-29, Satoh does not explicitly disclose the following limitations of the duration of the test pattern cycle period being narrowed, "wherein only for the first test pattern is narrowed, wherein for the first test pattern and for the plurality of test patterns is narrowed, and wherein for the plurality of test patterns is narrowed successively from the top pattern address throughout the entire test pattern in order".

However, Kurosaki (US 6,314,536), in analogous art, discloses a burst address producing circuit (8, Figure 1) capable of producing two burst address signals in one test period, which comprises a clock-repetition-rate doubling circuit 15 for outputting a clock at twice the pulse repetition rate of the test period signal TI, (see, Abstract). A timing chart showing waveforms and address signals produced in main elements of the memory testing apparatus 1 is illustrated in Figure 5. For example, Figure 5A shows a test period signal TI, and Figure 5D shows the burst address signals, having two burst address signals with respect to test period signal TI. Therefore, the cycle period rate of Figure 5D is narrower than the test period signal TI, by a factor of two.

It would have been obvious to a person having ordinary skill in the art at the time the invention was made to use the burst address producing circuit as taught by Kurosaki in the semiconductor testing apparatus of Satoh, for the purpose of testing a memory in the form of semiconductor integrated circuit, which adopts double data rate system and operates in burst mode, thus avoiding some of the drawbacks associated with the

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conventional memory testing, resulting in reduction of the throughput, and imposing heavy burden or load on programmers. The double data rate system provides a memory testing capable of supplying two address signals to a failure analysis memory in one test period, and hence capable of carrying out the test of memories at one time or within a shorter time period even in testing memories each operating in burst mode.

Regarding Claims 19-21, 30-32, Satoh does not explicitly disclose the following limitations of the duration of the test pattern cycle period being widened, "wherein the duration of the test pattern cycle period only for the first test pattern is widened, wherein the duration of the test pattern cycle period for the first test pattern and for the plurality of test patterns is widened, and wherein the duration of the test pattern cycle period for the plurality of test patterns is widened successively from the top pattern address throughout the entire test pattern in order".

However, in analogous art, Kurosaki (US 6,314,536) discloses a variable delay circuit 13, which delays a test period signal TI, and an address hold circuit 9, which holds the first address signal ADR0 as shown in Figure 2D until a next address signal is supplied, Figure 1.

It would have been obvious to a person having ordinary skill in the art at the time the invention was made to use the variable delay and hold circuits as taught by Kurosaki in the apparatus of Satoh, for the purpose of varying (widening) the pattern Test Period, since varying (widening) the Test Period results in memory testing flexibility by providing a slower clock for external test system compatibility.

Response to Arguments

Applicant's arguments, see Amendment, filed 3/30/2005, with respect to the rejection of claims 3 and 6-32 under 35 U.S.C. 102(e) as being anticipated by Kurosaki (US 6314536) have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground of rejection is made in view of rejection of Claims 3 and 6-32 under 35 U.S.C. 103(a) as being unpatentable over Satoh (U.S. Patent No. 6,477,672) in view of Kurosaki (U.S. Patent No. 6,314,536), as set forth in the present Office Action.

In reference to the phrase "such a manner" which renders the claim indefinite under 35 U.S.C. 112, second paragraph, the Applicant argues that the phrase "such a manner" has not been shown within MPEP 2173.05(c) to comply with 35 U.S.C. 112, second paragraph. In response to Applicant's argument, the Examiner notes the term "such a manner" is equivalent to the phrase "such as", which renders the claim indefinite because it is unclear whether the limitations following the phrase are part of the claimed invention. See MPEP § 2173.05(d).

In response to Applicant's argument that the objection to the claims for the use of the term "adapted to", is inconsistent with other actions taken by the Examiner, it is noted that the U.S. patents, cited by the Applicant, were previously issued by the Examiner under slightly different priorities, policies and procedures, as set forth by the Guidelines of the U.S. Patent Office.

Applicant's arguments with respect to the rejection of claims under prior art are moot in view of the new grounds of rejection.

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Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to JAMES C. KERVEROS whose telephone number is (571) 272-3824. The examiner can normally be reached on 9:00 AM TO 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on (571) 272-3819. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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Date: 1 June 2005
Office Action: Non-Final Rejection

JAMES C KERVEROS

Examiner
Art Unit 2133

By: 